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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,551	09/11/2006	Ingrid M. Verbauwhede	UCLARF:003NP	2110
29995 7590 03/19/2008 KNOBBE MARTENS OLSON & BEAR LLP 2040 MAIN STREET FOURTEENTH FLOOR IRVINE, CA 92614				
EXAMINER CHANG, DANIEL D				
ART UNIT 2819		PAPER NUMBER		
NOTIFICATION DATE 03/19/2008		DELIVERY MODE ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary

Application No.

10/565,551

Applicant(s)

VERBAUWHEDE ET AL.

Examiner

Daniel D. Chang

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 December 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) 21-25 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 5-11 and 14-20 is/are rejected.
- 7) ☒ Claim(s) 3, 4, 12 and 13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12/19/2007 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

Drawings

The drawings are objected to because a solid dot should be placed at the output node of the inverter on NOR side of OR-gate in Fig. 6; and the two n-type transistors at the bottom of the Fig. 10 should be connected to OUT and /OUT, respectively. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 1 and 8 are objected to because of the following informalities:

Claim 1 is missing a claim number, “1”.

Claim 8 is not quite clear as to what the limitation, "such that each node of said differential pull-down network both a first signal and an inverse of the first signal control a transistor that loads the node" refers to. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, and 5-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Jia et al. (US 6,633,188 B1, hereinafter "Jia").

Regarding claim 1, Jia discloses, in Figs. 1 and 2, an apparatus comprising:

a sense amplifier based logic gate (102 in Fig. 1) having an input network (276, 278), said input network comprising a differential pull-down network (276, 278) wherein, for a stable input combination, internal nodes (gates of 276, 278) of said differential pull-down network are provided to one or more output nodes (drains of 276, 278) of said differential pull-down network.

Regarding claim 2, Jia discloses that wherein said differential pull down network comprises a special differential pull down network (276 and 278 are considered to be special compared to some other less special differential pull down network).

Regarding claim 5, Jia discloses that wherein during evaluation a cross-coupled inverter (252, 270; 262, 272) toggles to one state and provides a stable output when said differential pull-down network provides a path to ground.

Regarding claim 6, Jia discloses a first transistor (281), which is always on (See 281 connected to V_{DD} in Fig. 1), configured to prevent a floating node by serving as a path for sub-threshold currents.

Regarding claim 7, Jia discloses differential output nodes (see drains of 276, 278) configured to provide differential signals to a differential input (sources of 270, 272).

Regarding claim 8, Jia discloses that wherein said differential pull-down network is configured such that each node of said differential pull-down network both a first signal (D) and an inverse (/D) of the first signal control a transistor (278, 276) that loads the node.

Regarding claim 9, Jia discloses a clocked transistor (see 250) provided between output nodes of said logic gate such that when a clock-signal becomes low, said clocked transistor provides charge stored at one output node to partially charge said output nodes and said internal nodes to an intermediate voltage (it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987)).

Claims 19 and 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Pearson et al. (US 5,909,127).

Regarding claim 19, see 302, 304, 306, and 308 in Fig. 4.

Regarding claim 20, see 902, 904, 906, and 908 in Fig. 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 10, 11, and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jia in view of Huang et al. ("New CMOS Differential Logic Circuits for True-Single-Phase Pipelined Systems", hereinafter, "Huang").

The teachings of Jia have been discussed above. Jia teaches sense amplifier with pull-down network but does not teach a sense amplifier with pull-up network

However, Huang teaches a sense amplifier with both pull-down (n-tree) and pull-up network (p-tree) wherein the sense amplifier with pull-up network is in upside down formation of a sense amplifier with pull-down network with different types of transistors.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have reversed the formation of the sense amplifier with pull-down network and types of transistors of Jia to the sense amplifier with pull-up network as taught by Huang in order to provide an inverted output at the sense amplifier output.

Allowable Subject Matter

Claims 3, 4, 12, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and correct the claim objections.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Daniel D. Chang/
Primary Examiner, Art Unit 2819